Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-17. (Cancelled)

18. (Currently Amended) A semiconductor device having, as its operation mode, a normal mode and a power down mode with smaller current consumption than that of said normal mode, comprising:

a first input path transmitting a first input signal ~~activated in said normal mode~~;

a second input path transmitting a second input signal ~~activated in said power down mode~~; and

an internal circuit operating in response to said first and second input signals, wherein

said first and second input signals are activated in said normal and power down modes, respectively, that do not occur at the same time ~~in respective time periods different from each other~~.

19. (Previously Presented) The semiconductor device according to claim 18 further comprising:

a memory array including a plurality of memory cells arranged in a matrix of rows and columns; and

a self-refresh control unit generating a self-refresh address in said power down mode, wherein

said first input signal corresponds to an address supplied in said normal mode,

said second input signal corresponds to said self-refresh address, and

said internal circuit includes an address decode circuit decoding either one of said first and second input signals and generating said first output signal for partially activating said memory array.

20. (Currently Amended) The semiconductor device according to claim 19, wherein said address decode circuit includes

a precharge circuit charging a common node to an initial potential,[[.]]

a first decode unit connected to said common node and receiving said first input signal, and

a second decode unit connected to said common node and receiving said second input signal.

21. (Previously Presented) The semiconductor device according to claim 18, wherein said internal circuit includes

a level conversion circuit converting respective amplitudes of said first and second input signals to provide a first output signal from a common node,

said level conversion circuit has

a first connection circuit provided on a first path connecting said common node to a ground node and rendered conductive in response to said first input signal, and

a second connection circuit provided on a second path, different from said first path, connecting said common node to the ground node, said second connection circuit being rendered conductive in response to said second input signal.

22. (Previously Presented) The semiconductor device according to claim 18, further comprising:

a control circuit outputting an internal control signal as said first input signal according to a command in said normal mode; and

a precharge circuit outputting said second input signal for fixing an internal node to which said internal control signal is transmitted at a power supply potential in said power down mode, wherein

said internal circuit has an input connected to said internal node.